

Appl. No. 10/709,568  
Amdt. dated January 18, 2007  
Reply to Office action of October 20, 2006

**Listing of Claims:**

1. (original) A bipolar junction transistor, comprising:

- a substrate;
  - a dielectric layer formed on the substrate;
  - 5 an opening formed in the dielectric layer to expose a portion of the substrate;
  - a semiconductor layer formed on a sidewall and a bottom of the opening, the semiconductor layer extending outside the opening and above the dielectric layer;
  - a spacer formed on the semiconductor layer to define a self-aligned emitter region in the opening;
  - 10 an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer; and
  - a salicide layer formed on the emitter conductivity layer and on the portion of the semiconductor layer extending outside the opening and above the dielectric layer.
  - 15
2. (original) The bipolar junction transistor of claim 1, wherein the semiconductor layer comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs.
- 20 3. (original) The bipolar junction transistor of claim 1, further comprising a selective implant collector region formed in the substrate beneath the semiconductor layer.
4. (original) The bipolar junction transistor of claim 1, further comprising an extended conductivity layer formed on the dielectric layer to connect to the semiconductor layer.
- 25 5. (original) The bipolar junction transistor of claim 4, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

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6. (original) The bipolar junction transistor of claim 4, wherein the extended conductivity layer is composed of polysilicon.

- 5 7. (original) A hetero-junction bipolar junction transistor, comprising:  
a substrate;  
a dielectric layer formed on the substrate;  
an opening formed in the dielectric layer to expose a portion of the substrate;  
a GaAs layer formed on a sidewall and a bottom of the opening;  
10 a spacer formed on the GaAs layer to define a self-aligned emitter region in the opening; and  
an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the GaAs layer.
- 15 8. (original) The hetero-junction bipolar junction transistor of claim 7, further comprising a selective implant collector region formed in the substrate beneath the GaAs layer.
9. (original) The hetero-junction bipolar junction transistor of claim 7, wherein the GaAs layer extends outside the opening and above the dielectric layer.
- 20 10. (original) The hetero-junction bipolar junction transistor of claim 9, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the GaAs layer extending outside the opening and above the dielectric layer.
- 25 11. (original) The hetero-junction bipolar junction transistor of claim 7, further comprising an extended conductivity layer formed on the dielectric layer to connect to the GaAs layer.

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12. (original) The hetero-junction bipolar junction transistor of claim 11, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

5 13. (original) The hetero-junction bipolar junction transistor of claim 11, wherein the extended conductivity layer is composed of polysilicon.

14. (original) A hetero-junction bipolar junction transistor, comprising:

- 10 a substrate;
- a dielectric layer formed on the substrate;
- an opening formed in the dielectric layer to expose a portion of the substrate;
- a InP layer formed on a sidewall and a bottom of the opening;
- a spacer formed on the InP layer to define a self-aligned emitter region in the opening; and
- 15 an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the InP layer.

15. (original) The hetero-junction bipolar junction transistor of claim 14, further comprising a selective implant collector region formed in the substrate beneath the InP  
20 layer.

16. (original) The hetero-junction bipolar junction transistor of claim 14, wherein the InP layer extends outside the opening and above the dielectric layer.

25 17. (original) The hetero-junction bipolar junction transistor of claim 16, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the InP layer extending outside the opening and above the dielectric layer.

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18. (original) The hetero-junction bipolar junction transistor of claim 14, further comprising an extended conductivity layer formed on the dielectric layer to connect to the InP layer.

5 19. (original) The hetero-junction bipolar junction transistor of claim 18, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

10 20. (original) The hetero-junction bipolar junction transistor of claim 18, wherein the extended conductivity layer is composed of polysilicon.

21. (original) A hetero-junction bipolar junction transistor, comprising:  
a substrate;  
a dielectric layer formed on the substrate;  
15 an opening formed in the dielectric layer to expose a portion of the substrate;  
an AlGaAs layer formed on a sidewall and a bottom of the opening;  
a spacer formed on the AlGaAs layer to define a self-aligned emitter region in the opening; and  
an emitter conductivity layer being filled into the self-aligned emitter region, and a  
20 PN junction being formed between the emitter conductivity layer and the AlGaAs layer.

22. (original) The hetero-junction bipolar junction transistor of claim 21, further comprising a selective implant collector region formed in the substrate beneath the AlGaAs layer.

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23. (original) The hetero-junction bipolar junction transistor of claim 21, wherein the AlGaAs layer extends outside the opening and above the dielectric layer.

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24. (original) The hetero-junction bipolar junction transistor of claim 23, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the AlGaAs layer extending outside the opening and above the dielectric layer.

5 25. (original) The hetero-junction bipolar junction transistor of claim 21, further comprising an extended conductivity layer formed on the dielectric layer to connect to the AlGaAs layer.

10 26. (original) The hetero-junction bipolar junction transistor of claim 25, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

27. (original) The hetero-junction bipolar junction transistor of claim 25, wherein the extended conductivity layer is composed of polysilicon.

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